Independent claims 1 recites in part "a serial-to-parallel converter receiving the clock signal, the mode signal and serial data, and converting the serial data into parallel data." Also, independent claim 16 recites in part "a parallel-to-serial converter receiving the clock signal, the mode signal and parallel data, and converting the parallel data into serial data." Neither Walters nor Hoffer discloses or suggests at least these claimed features.

The Examiner admitted that Walters fails to show a selection of a clock signal in response to a mode signal (see p. 3, lines 1-2 of the June 15, 2000 Office Action). Then it must be that the Walters cannot disclose or suggest either a serial-to-parallel converter or a parallel-to-serial converter receiving the clock signal and converting the data, respectively.

Hoffert fails to cure at least these deficiencies of Walter. Applicant notes that Hoffert is merely concerned with processing video data. Hoffert discloses that on every rising edge of the clock VSCLK 20, 128 bits of pixel data from the frame buffer 12 are loaded on to the video bus 15. The pixel data is then processed by the memory display interface (MDI) 14.

Hoffert is silent whether any parallel data is converted to serial data or vice versa. Thus, Hoffert fails to disclose or suggest the features of claims 1 and 16 as recited above.

Because neither Walters nor Hoffert discloses or suggests the features as claimed above, the combination of Walters and Hoffert also fails to disclose or suggest at least the same features.

Also, it is a fundamental tenet of patent law that the teachings of each piece of applied art must be taken as a whole. When taken as a whole, it is illogical to combine Walters and Hoffert since they teach away from each other. Thus any rejection based on a combination of Walters and Hoffert is improper.

In the Office Action, the Examiner indicated that Hoffert discloses generating clock signals 73-75 at frequencies required for 32, 16, and 8 bit modes, and selecting one of the clock signals (p. 3, lines 2-5 of the June 15, 2000 Office Action). The Examiner then went on to merely declare that it would have been obvious modify Walters as taught by Hoffert to arrive at the claimed inventions. Applicant disagrees.

First, it is noted that VSCLK is generated by selecting one of the clock signals 73-75 (column 6, lines 29-35 of Hoffert). The only purpose of this clock is to synchronize the delivery of pixel data from the frame buffer 12 to MDI 14.

As noted above, on every rising edge of the VSCLK 20, 128 bits of pixel data from the frame buffer 12 are loaded on to the video bus 15 to be processed by the MDI 14. Thus if the pixel depth is 32 bits, then data for 4 pixels can be loaded on to the video bus 15. Likewise, if the pixel depth is 16 or 8 bits, then data for 8 or 16 pixels can be loaded (column 3, lines 23-27).

However, the MDI 14 is only able to process data for 4 pixels simultaneously regardless of the pixel depth modes (column 3, lines 48-53). Thus if the pixel depth is 32 bits, then the VSCLK 20 may be as fast as the pipeline clock 28 (column 4, lines 43-45), which controls the timing of the pixel data processing, since there are only data for 4 pixels on the video bus 15. On

the other hand, if the depth is 16 or 8 bits, then there are data for 8 or 16 pixels on the bus. Consequently, VSCLK 20 must be slowed by half or by a quarter to provide enough time to process all pixel data loaded onto the video bus 15. In short, Hoffert depends on either slowing down or speeding up the clock signal to provide the necessary synchronization.

Walters uses a different mechanism to synchronize data transfers. Walters does NOT depend on adjusting the frequency of the clock to synchronize. As shown in the Response filed on May 12, 2000, none of the signals SR CLK 32, CLOCK 29, CNTR CLK 48 are generated based on the length of data (see also Figs. 1 and 10 of Walters).

It was also explained (in the previous response) that Walters uses the length parameters L1 and L0 to determine the number of time the shift registers 20 and 120 are to be shifted (column 3, line 39-43 of Walters). When the shift registers are shifted an appropriate number of times, such as 16 or 8, data transfer is complete. This method of synchronization is independent of the frequency of the clock signals. It is clear that the Walters and Hoffert mechanisms for synchronization are completely different from, and inconsistent with, each other, i.e., they teach away from each other.

For at least the reasons stated above, independent claims 1 and 16 are not rendered obvious by the combination of Walters and Hoffert.

Claims 2-15 and 17-34 depend from independent claims 1 and 16. Therefore, these dependent claims are also not rendered obvious by the

combination of Walters and Hoffert for at least the reasons stated with respect to claims 1 and 16.

Applicant respectfully requests the Examiner to withdraw this Section 103 rejection of claims 1-34 Walters and Hoffert.

CONCLUSION

For the foregoing reasons, Applicants respectfully requests the Examiner to withdraw all of the objections and rejections.

Should there be any outstanding matters which need to be resolved in the present application, the Examiner is respectfully requested to contact Hyung Sohn (Registration No. 44,346) at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment from or credit any overpayment to

Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §1.16 or under 37 C.F.R. §1.17; particularly, the extension of time fees.

Respectfully submitted,

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